Design and Simulation of a Nanoscale Threshold-Logic Multiplier

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Abstract **–Multiplication is one of the most important operations in microprocessors and digital signal processing systems. Different multiplier architectures have been proposed in the literature. One of the most widely used architecture is the Wallace tree multiplier. This multiplier is known for its high speed. However, it occupies a large area. In this paper, we used Threshold Logic Gates instead of conventional logic gates to reduce the area. The multiplier was designed in 65nm CMOS technology, and achieved 28% reduction in the number of transistors compared to the one with conventional logic gates. It also achieved a lower power-delay-product.**

Keywords **– Multiplier, adder, Threshold logic gates.**

1. Introduction

Multiplication is an important operation, and its speed dominates the performance of many computational systems. Multiplication is less common than addition, but is still essential for microprocessors, digital signal processors, and graphic engines [1]. Multipliers are generally classified in two major categories, which are the array and tree multipliers. Each category includes different types, with various structures, types of adders, or logic gates. Each type has its own advantages and disadvantages, based on its speed, power consumption, and area [2].

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One of the widely-used fast multipliers is the Wallace tree multiplier, which was modified and enhanced by many research groups. In [3], a new Wallace tree multiplier was designed with a modified carry-select adder to reduce the area. In other designs, full adder and half adder were used to improve the performance as detailed in [4] and [5].

Basically, multiplication operation depends on addition. Adders are widely used digital components and they are necessary parts of microprocessors. Two types of adders can be used in multipliers: half adders and full adders. These adders can be designed using conventional logic gates or threshold logic gates. The threshold logic gates are unique types of gates in which the weighted sum of the inputs is compared with a threshold value. If the weighted sum is larger than the threshold, the output will be high, otherwise it will be low [6]. The main advantage of these gates is that they use fewer transistors to implement logic functions compared to conventional logic gates. Threshold logic gates have been used to realize many applications such as adders [7], multipliers [8], and decoders [9].

2. Wallace tree multiplier

Wallace tree multiplier is a very effective and popular multiplier. Its architecture is divided into three stages. The first stage implements the generation of partial products which is the common and most important stage in a multiplier. In this stage, N^2 AND gates are required, where N is the number of bits. In the second stage, the Wallace-tree particular feature is recognized, which is the accumulation of partial products. The accumulation is performed using full adders and half adders. The full adder is known as a (3:2) compressor because of its ability to add 3 bits from a single column of the partial product matrix and output 2 bits. In this stage, all partial products are summed up according to the type of Wallace-tree multiplier, and the output is arranged into two rows. The last stage is the final addition in which the summation of the two rows coming from the previous stage is performed. As indicated previously, the design of this multiplier is based on adders, which have various

implementations. In this paper, we considered the threshold logic implementation which is explained in the following section.

3. Design of threshold logic adders

Threshold logic adders comprise only two threshold logic gates: the majority gate and the (1,1,1,2) gate [10]. These gates could be designed using different techniques including the wired-inverters. Using this method, each gate is designed with several inverters connected together, and their output is connected to an output inverter. Each input is connected to an inverter. Then the output of the wired-inverter goes to a Buffer. Figure 1. shows the output-wired inverter design of the (1,1,1,2) gate, which implements the SUM function, with five inputs and one output [10]:

$$Sum = a + b + cin + 2\ cout' - 2.5$$

All gates have the same structure, and the different functions are implemented using different transistor sizes. Each inverter consists of one PMOS transistor and one NMOS transistor. When the input is low, PMOS is ON and NMOS is OFF. Therefore, PMOS acts like a resistance R_p and NMOS acts like an open circuit. When the input is high, NMOS is ON and PMOS is OFF. Thus, NMOS acts like a resistance R_n and PMOS acts like an open circuit. The values of these resistors depend on the transistor size, and determine the input voltage to the buffer. If this voltage is high, the buffer output will be low, and *vice-versa*.

In our design, all the needed threshold gates were designed and simulated using PTM 65nm CMOS transistor models [11]. First the gates were designed and simulated. Then, the designed gates were used to build the half and full adders. Finally, the adders were connected to build a 4×4 multiplier.

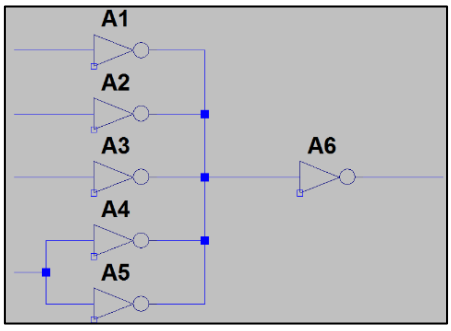

Figure 1. Output-wired inverters threshold logic gate

4. Multiplier design

Conventional Wallace tree multiplier is designed in three stages:

a. Partial Product Generation.
b. Grouping of Partial Product.
c. Final Addition

In particular, the design of a 4×4 Conventional Wallace tree multiplier was performed as follows. The first step was to design the partial products (PP) generator, which consists of 16 AND gates for a 4 bit multiplier. The 4 bits of multiplicand and the 4 bits of multiplier go to AND gates to produce the partial products. The design of PP generator is shown in Figure 2.

- {a0, a1, a2, a3, b0, b1, b2, b3} are the inputs (multiplicand and multiplier).
- {S00, S01, S02, S03, S10, S11, S12, S13, S20, S21, S22, S23, S30, S31, S32, S33} are the outputs of this stage which are the inputs of the next stage.

Figure 3. shows the design of the second stage in conventional multiplier. It is the reduction of PPs. In this stage some of the PP generated in the previous stage will be summed using four Full adders and two Half adders to produce the groups which will go directly to the last stage.

- {S02, S03, S11, S12, S13, S21, S22, S23, S30, S31, S32} are the inputs.
- {G4, G5, G6, G7, G8, G9, G10, G11} are the outputs of this stage which are the inputs of the next stage.

Figure 4. shows the third and the last stage in conventional multiplier, which is the final addition. In this stage, the groups produced from the second stage are summed with the rest of the PPs left from the first stage.

- {G1(S01), G2(S10), G3(S20), G4, G5, G6, G7, G8, G9, G10, G11, G12(S33)} are the inputs.
- {P1, P2, P3, P4, P5, P6, P7} are the outputs of this stage which are the final products.

After connecting all three stages together, the complete multiplier is produced as shown in Figure 5. The multiplicand and multiplier enter the first stage and go through the three stages to produce the final product.

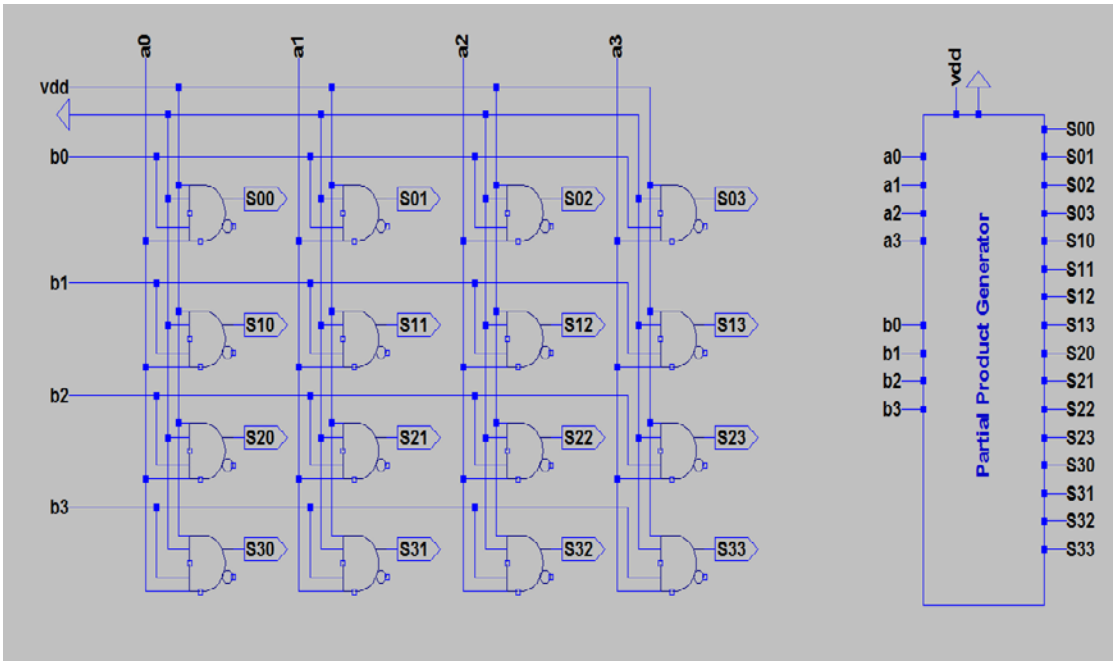

Figure 2. Partial product generator

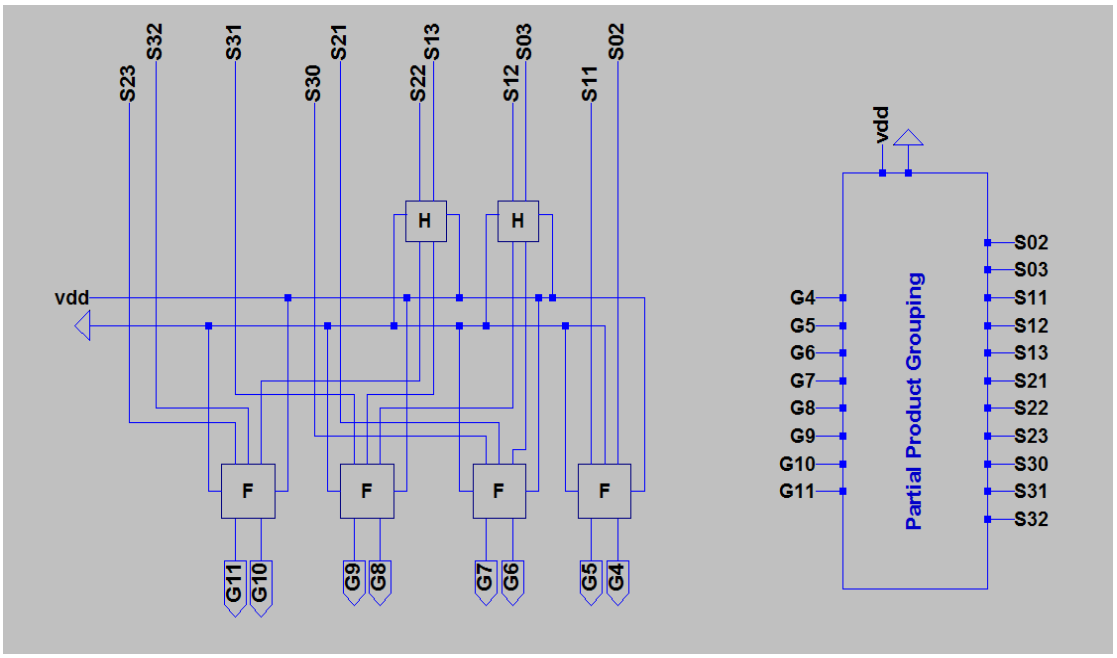

Figure 3. Partial product grouping

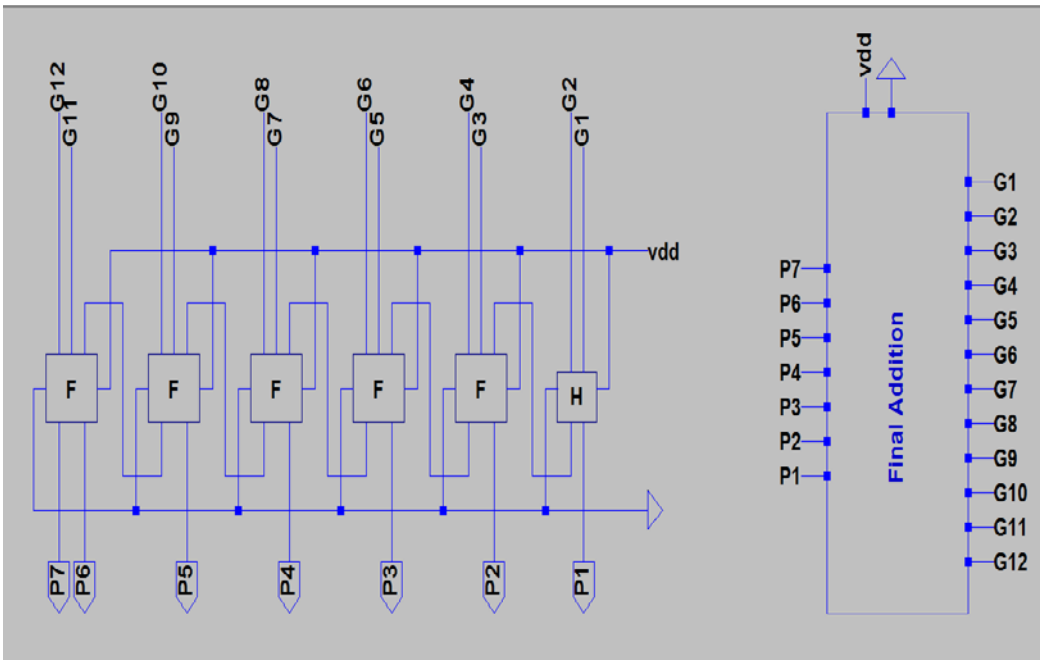

Figure 4. Final addition

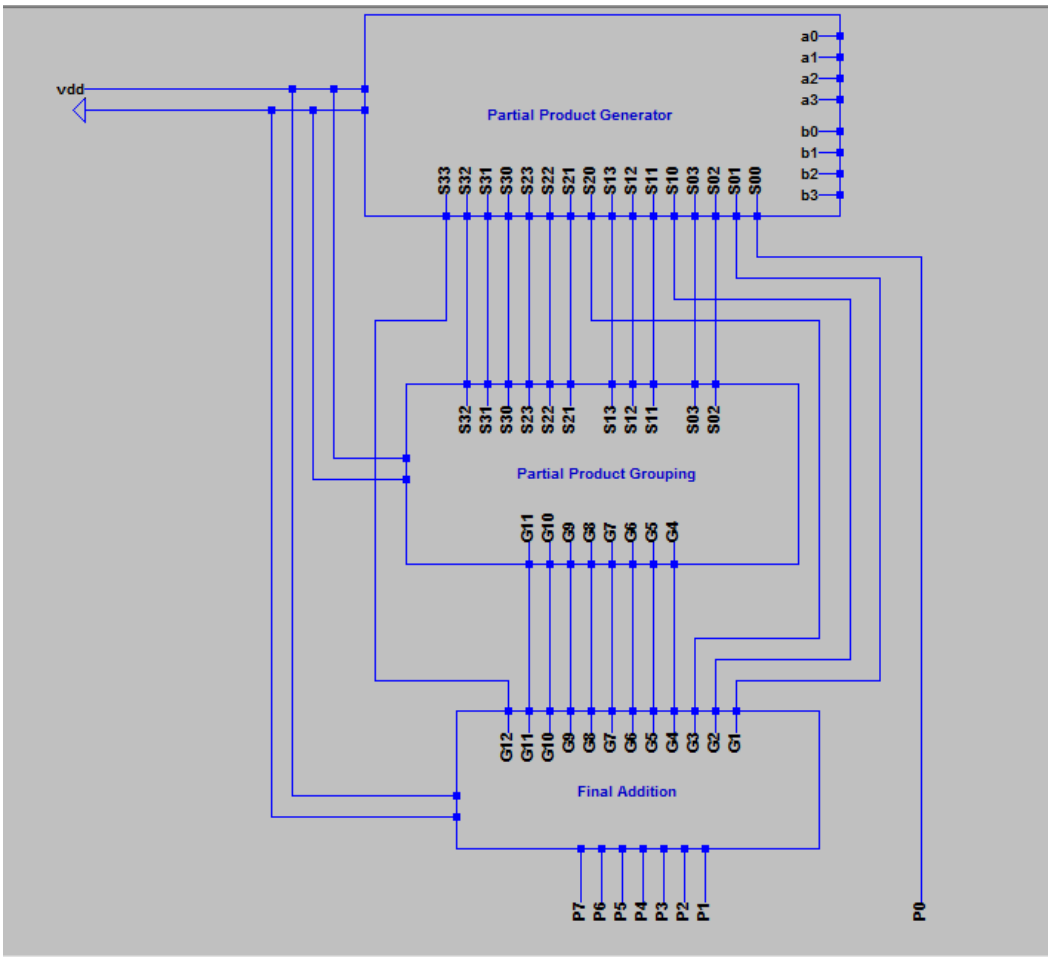

Figure 5. Wallace tree multiplier

5. Results

After connecting all the components, the multiplier was produced and simulated. The simulation results are shown in Fig. 6. & 7. These results proved proper functionality of the multiplier.

Once the functionality was verified, this threshold logic multiplier was compared with a similar multiplier that was designed with conventional logic gates [5]. Table 1. shows the total numbers of components used for designing these two multipliers. One of the disadvantages of the Wallace multiplier is that it requires more hardware. However, using threshold gates reduced the total number of transistors by 28%.

Power consumption and delay are the most important parameters that measure the quality of the designed multiplier. The final stage time delay is the greatest, because there can be delays as the carriers are propagated in the final addition. The delay and power consumption were found by simulating the multiplier, and the power-delay-product (PDP) was calculated. These characteristics were compared with those of the multiplier presented in [5], as summarized in Table 2. The results show that the threshold-logic multiplier is faster than the conventional-gate multiplier, though it consumes more power. However, the overall PDP of the threshold-logic multiplier is significantly lower than that of the conventional-gate multiplier.

Table 1. Number of components

	Multiplier with threshold logic gates	Multiplier with conventional logic gates
Total number of AND gates	16	16
Total number of half adders	3	3
Total number of full adders	9	9
Total number of PMOS transistors	180	249
Total number of NMOS transistors	180	249

Table 2. Multiplier characteristics

	Multiplier with threshold logic gates	Multiplier with conventional logic gates
Power (mW)	2.2	0.7
Delay (μs)	0.0004	50
PDP (nJ)	0.0009	35

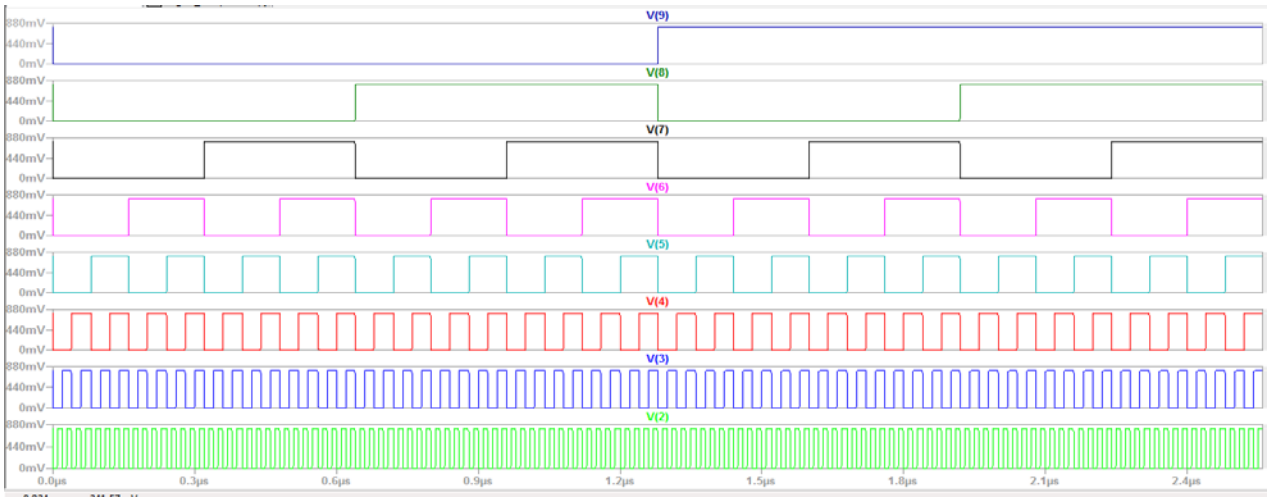

Figure 6. Multiplier inputs

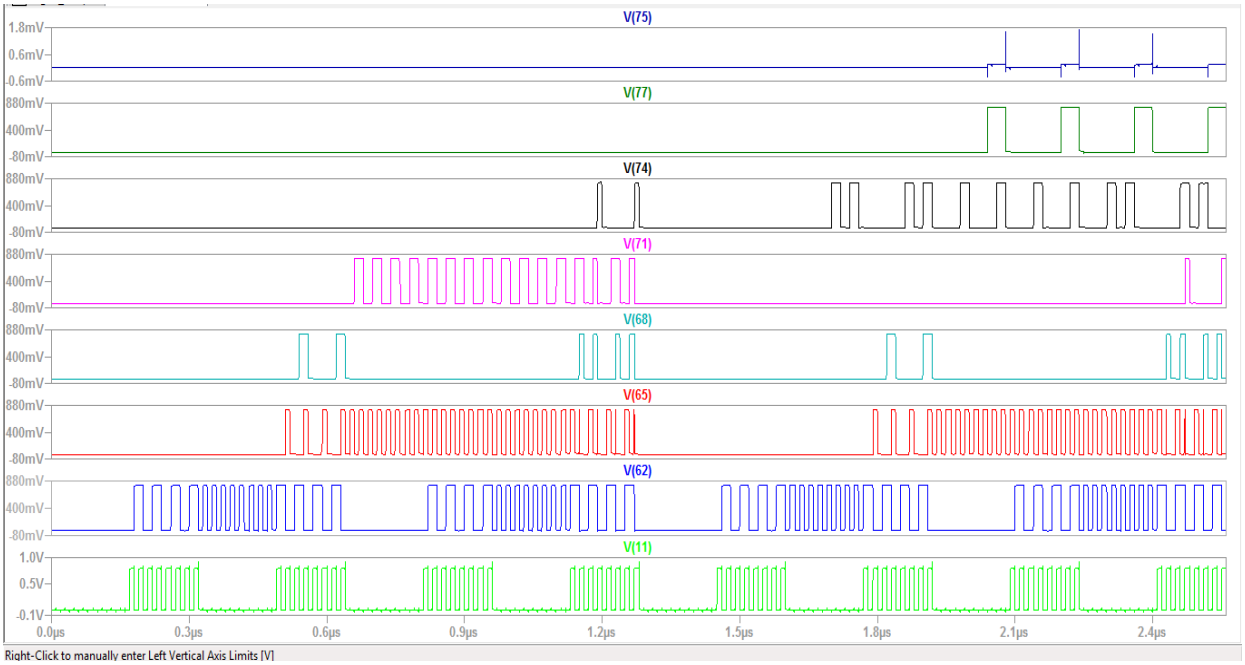

Figure 7. Multiplier outputs

6. Conclusion

This paper presented the design and simulation of a 65 nm CMOS Wallace tree multiplier. The design was based on threshold logic gates, which were used to reduce the number of transistors, hence the area of the multiplier. The threshold gates were implemented with output-wired inverters, and the functions were differentiated by the transistor sizes. This 65 nm multiplier comprised 28% less transistors compared to the one that uses conventional logic gates. It is also characterized by 2.2 mw power consumption, 0.4 ns delay and 0.9 pJ PDP. This PDP is significantly smaller compared to the Wallace-tree multiplier which was designed using conventional logic gates.

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